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Jameco Part Number 41339

# Am9016

## 16,384 x 1 Dynamic R/W Random Access Memory
## Advanced MOS/LSI

### DISTINCTIVE CHARACTERISTICS

- High density 16K x 1 organization
- Replacement for MK4116
- Low maximum power dissipation – 462mW active, 20mW standby
- High-speed operation – 150ns access, 320ns cycle (COM'L)
  200ns access, 375ns cycle (MIL)
- ±10% tolerance on standard +12, +5, −5 voltages
- TTL compatible interface signals
- Three-state output
- $\overline{RAS}$ only, RMW and Page mode clocking options
- 128 cycle refreshing
- Unlatched data output
- Standard 16-pin, .3 inch wide dual-in-line package
- JEDEC standard 18-pin, Chip-Pak™ leadless chip carrier
- Double poly N-channel silicon gate MOS technology
- Extended ambient operating temperature (−55 to +85°C) available

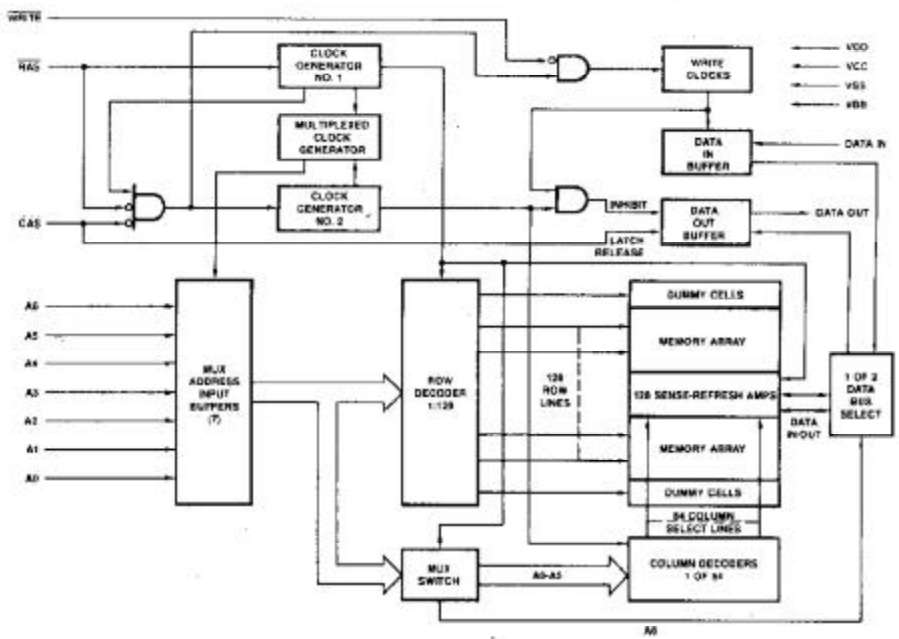
### GENERAL DESCRIPTION

The Am9016 is a high-speed, 16K-bit, dynamic, read/write random access memory. It is organized as 16,384 words by 1 bit per word and is packaged in a standard 16-pin DIP or 18-pin leadless chip carrier. The basic memory element is a single transistor cell that stores charge on a small capacitor. This mechanism requires periodic refreshing of the memory cells to maintain stored information.

All input signals, including the two clocks, are TTL compatible. The Row Address Strobe ($\overline{RAS}$) loads the row address and the Column Address Strobe ($\overline{CAS}$) loads the column address. The row and column address signals share seven input lines. Active cycles are initiated when $\overline{RAS}$ goes low, and standby mode is entered when $\overline{RAS}$ goes high. In addition to normal read and write cycles, other types of operations are available to improve versatility, performance and power dissipation.

The 3-state output buffer turns on when the column access time has elapsed and turns off after $\overline{CAS}$ goes high. Input and output data are the same polarity.

### BLOCK DIAGRAM

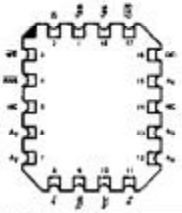



MOS-190

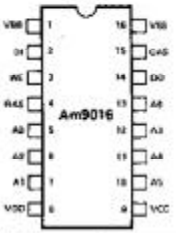
Chip-Pak is a trademark of Advanced Micro Devices, Inc.

## CONNECTION DIAGRAMS – Top Views

Chip-Pak
L-18-2



DIP




| | |
|---|---|
| A0 – A6 | ADDRESS INPUTS |
| $\overline{CAS}$ | COLUMN ADDRESS STROBE |
| DI | DATA IN |
| DO | DATA OUT |
| $\overline{RAS}$ | ROW ADDRESS STROBE |
| VDD | POWER (+12V) |
| VCC | POWER (+5V) |
| VSS | GROUND |
| VBB | POWER (−5V) |
| $\overline{WE}$ | WRITE ENABLE |

MOS 670

## MAXIMUM RATINGS above which useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65 to −150°C |
| Ambient Temperature with Power Applied | −55 to +85°C |
| Voltage on Any Pin Relative to VBB | 0.5 to +20V |
| VDD and VCC Supply Voltages with Respect to VSS | −1.0 to +15.0V |
| VBB − VSS (VDD − VSS > 0V) | 0V |
| Power Dissipation | 1.0W |
| Short Circuit Output Current | 50mA |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{DD}$ | $V_{CC}$ | $V_{SS}$ | $V_{BB}$ |
|---|---|---|---|---|---|
| Am9016DC/PC/LC | $0°C \le T_A \le +70°C$ | +12V ±10% | +5V ±10% | 0 | −5V ±10% |
| Am9016DL/LL | $-55°C \le T_A \le +85°C$ | +12V ±10% | +5V ±10% | 0 | −5V ±10% |

## ELECTRICAL CHARACTERISTICS over operating range (Notes 1, 9)

| Parameters | Description | | Test Conditions | Am9016 Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| VOH | Output HIGH Voltage | | IOH = −5.0mA | 2.4 | | VCC | Volts |
| VOL | Output LOW Voltage | | IOL = 4.2mA | VSS | | 0.40 | Volts |
| VIH | Input HIGH Voltage for Address, Data In | | | 2.4 | | 7.0 | Volts |
| VIHC | Input HIGH Voltage for $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$ | | | 2.7 | | 7.0 | Volts |
| VIL | Input LOW Voltage | | | −1.0 | | 0.80 | Volts |
| IIX | Input Load Current | | VSS ≤ VI ≤ 7V | −10 | | 10 | µA |
| IOZ | Output Leakage Current | | VSS ≤ VO ≤ VCC, Output OFF | −10 | | 10 | µA |
| ICC | VCC Supply Current | | Output OFF (Note 4) | −10 | | 10 | µA |
| IBB | VBB Supply Current, Average | $0°C \le T_A \le +70°C$ | Standby, $\overline{RAS} \ge$ VIHC | | | 100 | µA |
| | | $-55°C \le T_A \le +85°C$ | | | | 200 | |
| | | $0°C \le T_A \le +70°C$ | Operating, Minimum Cycle Time | | | 200 | |
| | | $-55°C \le T_A \le +85°C$ | | | | 400 | |
| IDD | VDD Supply Current, Average | Operating IDD1 | $\overline{RAS}$ Cycling, $\overline{CAS}$ Cycling, Minimum Cycle Times | | | 35 | mA |
| | | Page Mode IDD4 | $\overline{RAS} \le$ VIL, $\overline{CAS}$ Cycling, Minimum Cycle Times | | | 27 | |
| | | $\overline{RAS}$ Only Refresh IDD3 | $\overline{RAS}$ Cycling, $\overline{CAS} \ge$ VIHC, Minimum Cycle Times | | | 27 | |
| | $0°C \le T_A \le +70°C$ | Standby IDD2 | $\overline{RAS} \ge$ VIHC | | | 1.5 | |
| | $-55°C \le T_A \le +85°C$ | | $\overline{RAS} \ge$ VIHC | | | 2.25 | |
| CI | Input Capacitance | $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Inputs at 0V, f = 1MHz, Nominal Supply Voltages | | | 10 | pF |
| | | Address, Data In | | | | 5.0 | |
| CO | Output Capacitance | | Output OFF | | | 7.0 | |

## SWITCHING CHARACTERISTICS over operating range (Notes 2, 3, 5)

| Parameters | Description | | Am9016C Min | Am9016C Max | Am9016D Min | Am9016D Max | Am9016E Min | Am9016E Max | Am9016F Min | Am9016F Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| tAR | $\overline{RAS}$ LOW to Column Address Hold Time | | 200 | | 160 | | 120 | | 95 | | ns |
| tASC | Column Address Setup Time | 0°C ≤ $T_A$ ≤ +70°C | −10 | | −10 | | −10 | | −10 | | ns |
| | | −55°C ≤ $T_A$ ≤ +85°C | 0 | | 0 | | 0 | | NA | | ns |
| tASR | Row Address Setup Time | | 0 | | 0 | | 0 | | 0 | | ns |
| tCAC | Access Time from $\overline{CAS}$ (Note 6) | | | 185 | | 165 | | 135 | | 100 | ns |
| tCAH | $\overline{CAS}$ LOW to Column Address Hold Time | | 85 | | 75 | | 55 | | 45 | | ns |
| tCAS | $\overline{CAS}$ Pulse Width | 0°C ≤ $T_A$ ≤ +70°C | 185 | 10,000 | 165 | 10,000 | 135 | 10,000 | 100 | 10,000 | ns |
| | | −55°C ≤ $T_A$ ≤ +85°C | 185 | 5000 | 165 | 5000 | 135 | 5000 | NA | NA | ns |
| tCP | Page Mode $\overline{CAS}$ Precharge Time | | 100 | | 100 | | 80 | | 60 | | ns |
| tCRP | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 0°C ≤ $T_A$ ≤ +70°C | −20 | | −20 | | −20 | | −20 | | ns |
| | | −55°C ≤ $T_A$ ≤ +85°C | 0 | | 0 | | 0 | | NA | | ns |
| tCSH | $\overline{CAS}$ Hold Time | | 300 | | 250 | | 200 | | 150 | | ns |
| tCWD | $\overline{CAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9) | | 145 | | 125 | | 95 | | 70 | | ns |
| tCWL | $\overline{WE}$ LOW to $\overline{CAS}$ HIGH Setup Time | | 100 | | 85 | | 70 | | 50 | | ns |
| tDH | $\overline{CAS}$ LOW or $\overline{WE}$ LOW to Data In Valid Hold Time (Note 7) | | 85 | | 75 | | 55 | | 45 | | ns |
| tDHR | $\overline{RAS}$ LOW to Data In Valid Hold Time | | 200 | | 160 | | 120 | | 95 | | ns |
| tDS | Data In Stable to $\overline{CAS}$ LOW or $\overline{WE}$ LOW Setup Time (Note 7) | | 0 | | 0 | | 0 | | 0 | | ns |
| tOFF | $\overline{CAS}$ HIGH to Output OFF Delay | | 0 | 60 | 0 | 60 | 0 | 50 | 0 | 40 | ns |
| tPC | Page Mode Cycle Time | | 295 | | 275 | | 225 | | 170 | | ns |
| tRAC | Access Time from $\overline{RAS}$ (Note 6) | | | 300 | | 250 | | 200 | | 150 | ns |
| tRAH | $\overline{RAS}$ LOW to Row Address Hold Time | | 45 | | 35 | | 25 | | 20 | | ns |
| tRAS | $\overline{RAS}$ Pulse Width | 0°C ≤ $T_A$ ≤ +70°C | 300 | 10,000 | 250 | 10,000 | 200 | 10,000 | 150 | 10,000 | ns |
| | | −55°C ≤ $T_A$ ≤ +85°C | 300 | 5000 | 250 | 5000 | 200 | 5000 | NA | NA | ns |
| tRC | Random Read or Write Cycle Time | | 460 | | 410 | | 375 | | 320 | | ns |
| tRCD | $\overline{RAS}$ LOW to $\overline{CAS}$ LOW Delay (Note 6) | | 35 | 115 | 35 | 85 | 25 | 65 | 20 | 50 | ns |
| tRCH | Read Hold Time | | 0 | | 0 | | 0 | | 0 | | ns |
| tRCS | Read Setup Time | | 0 | | 0 | | 0 | | 0 | | ns |
| tREF | Refresh Interval | | | 2 | | 2 | | 2 | | 2 | ms |
| tRMW | Read Modify Write Cycle Time | | 600 | | 500 | | 405 | | 320 | | ns |
| tRP | $\overline{RAS}$ Precharge Time | | 150 | | 150 | | 120 | | 100 | | ns |
| tRSH | $\overline{CAS}$ LOW to $\overline{RAS}$ HIGH Delay | | 185 | | 165 | | 135 | | 100 | | ns |
| tRWC | Read/Write Cycle Time | | 525 | | 425 | | 375 | | 320 | | ns |
| tRWD | $\overline{RAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9) | | 260 | | 210 | | 160 | | 120 | | ns |
| tRWL | $\overline{WE}$ LOW to $\overline{RAS}$ HIGH Setup Time | | 100 | | 85 | | 70 | | 50 | | ns |
| tT | Transition Time | | 3 | 50 | 3 | 50 | 3 | 50 | 3 | 35 | ns |
| tWCH | Write Hold Time | | 85 | | 75 | | 55 | | 45 | | ns |
| tWCR | $\overline{RAS}$ LOW to Write Hold Time | | 200 | | 160 | | 120 | | 95 | | ns |
| tWCS | $\overline{WE}$ LOW to $\overline{CAS}$ LOW Setup Time (Note 9) | 0°C ≤ $T_A$ ≤ +70°C | −20 | | −20 | | −20 | | −20 | | ns |
| | | −55°C ≤ $T_A$ ≤ +85°C | 0 | | 0 | | 0 | | NA | | |
| tWP | Write Pulse Width | | 85 | | 75 | | 55 | | 45 | | ns |

Notes:
1. All voltages referenced to VSS.
2. Signal transition times are assumed to be 5ns. Transition times are measured between specified high and low logic levels.
3. Timing reference levels for both input and output signals are the specified worst-case logic levels.
4. VCC is used in the output buffer only. ICC will therefore depend only on leakage current and output loading. When the output is ON and at a logic high level, VCC is connected to the Data Out pin through an equivalent resistance of approximately 135Ω. In standby mode VCC may be reduced to zero without affecting stored data or refresh operations.
5. Output loading is two standard TTL loads plus 100pF capacitance.
6. Both $\overline{RAS}$ and $\overline{CAS}$ must be low read data. Access timing will depend on the relative positions of their falling edges. When tRCD is less than the maximum value shown, access time depends on $\overline{RAS}$ and tRAC governs. When tRCD is more than the maximum value shown access time depends on $\overline{CAS}$ and tCAC governs. The

Notes (Cont.)

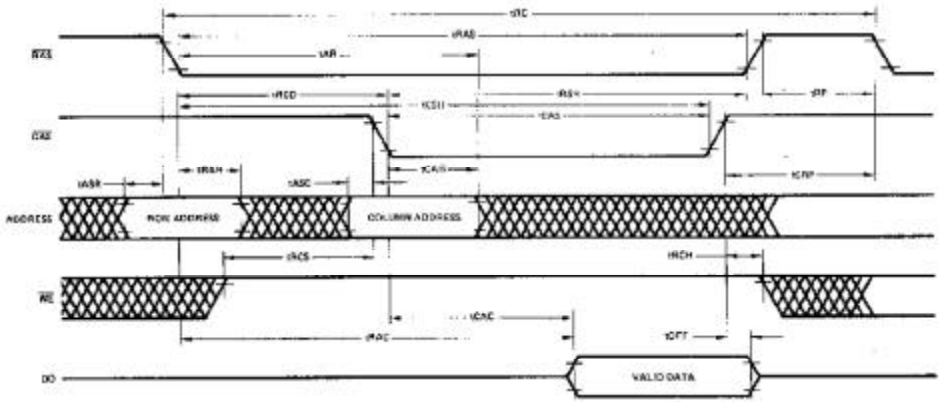
maximum value listed for tRCD is shown for reference purposes only and does not restrict operation of the part.

7. Timing reference points for data input setup and hold times will depend on what type of write cycle is being performed and will be the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
8. At least eight initialization cycles that exercise $\overline{RAS}$ should be performed after power-up and before valid operations are begun.
9. The tWCS, tRWD and tCWD parameters are shown for reference purposes only and do not restrict the operating flexibility of the part.

When the falling edge of $\overline{WE}$ follows the falling edge of $\overline{CAS}$ by at most tWCS, the data output buffer will remain off for the whole cycle and an "early write" cycle is defined. When the falling edge of $\overline{WE}$ follows the falling edges of $\overline{RAS}$ and $\overline{CAS}$ by at least tRWD and tCWD respectively, the Data Out from the addressed cell will be valid at the access time and a "read/write" cycle is defined. The falling edge of $\overline{WE}$ may also occur at intermediate positions, but the condition and validity of the Data Out signal will not be known.

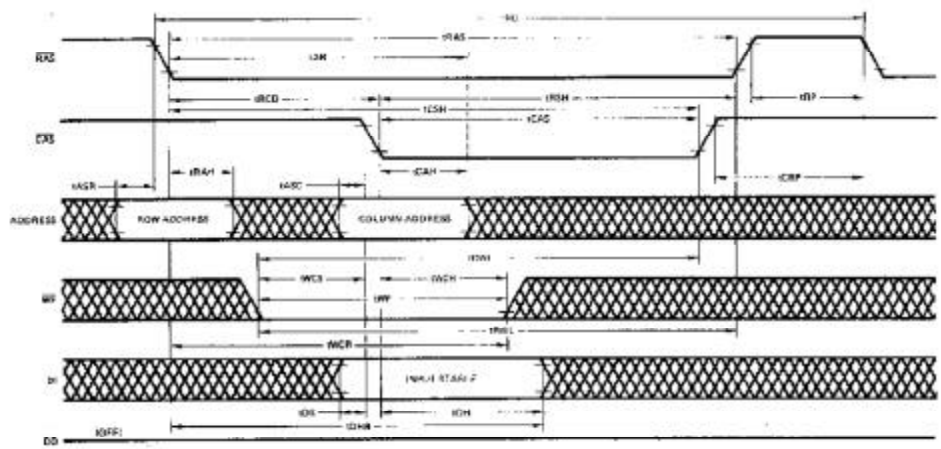
## SWITCHING WAVEFORMS

### READ CYCLE




MOS-192

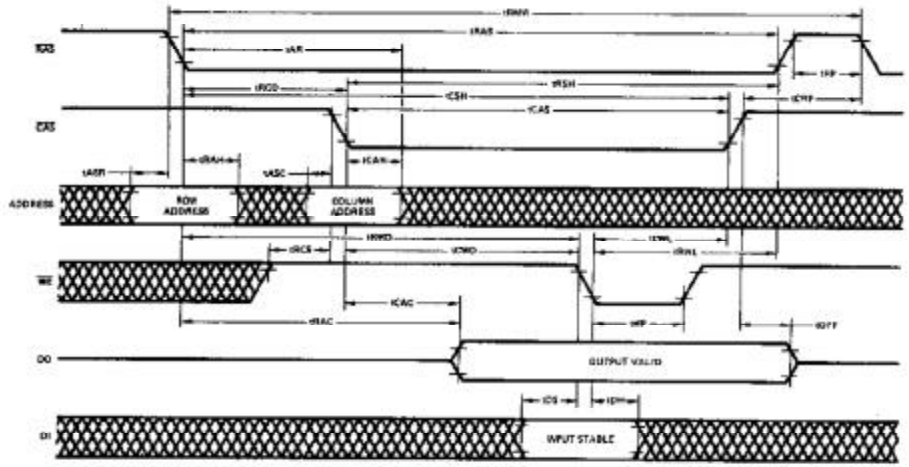
### WRITE CYCLE (EARLY WRITE)




MOS-193

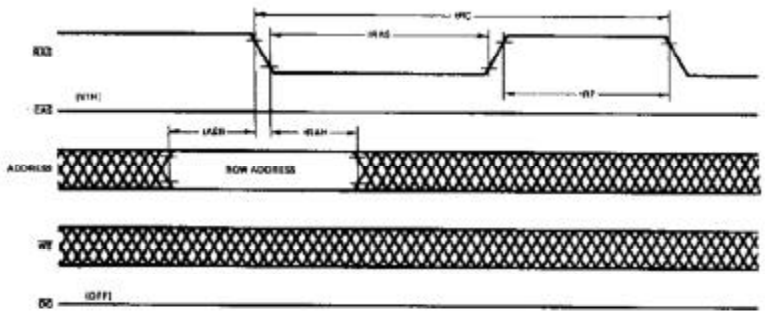
## SWITCHING WAVEFORMS (Cont.)

### READ-WRITE/READ-MODIFY-WRITE CYCLE



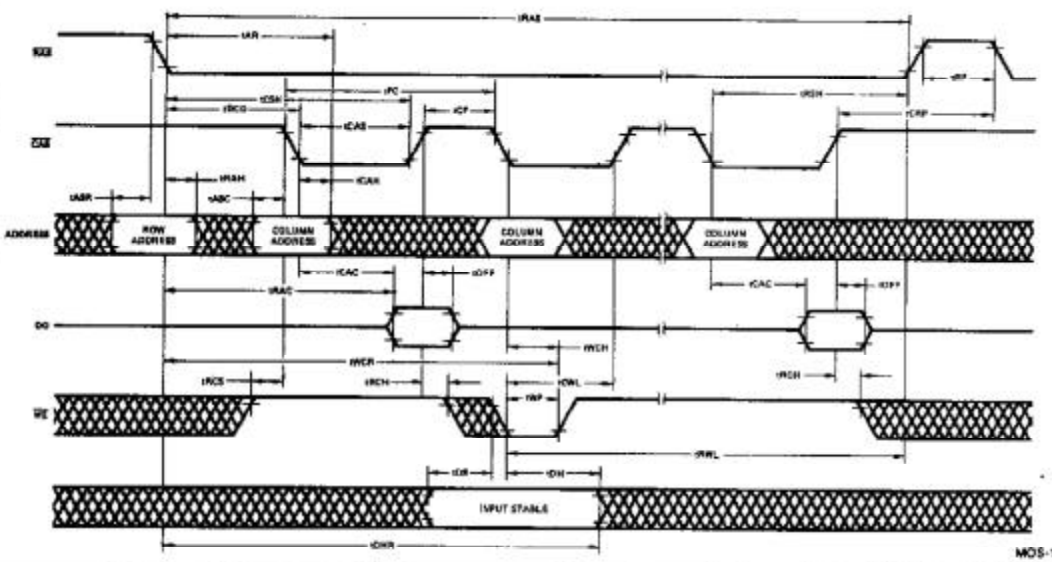

MOS-194

### $\overline{RAS}$ ONLY REFRESH CYCLE




MOS-195

### PAGE MODE CYCLE




MOS-196

4

## APPLICATION INFORMATION

The Am9016 electrical connections are such that if power is applied with the device installed upside down it will be permanently damaged. Precautions should be taken to avoid this mishap.

### OPERATING CYCLES

Random read operations from any location hold the $\overline{WE}$ line high and follow this sequence of events:

1) The row address is applied to the address inputs and $\overline{RAS}$ is switched low.
2) After the row address hold time has elapsed, the column address is applied to the address inputs and $\overline{CAS}$ is switched low.
3) Following the access time, the output will turn on and valid read data will be present. The data will remain valid as long as $\overline{CAS}$ is low.
4) $\overline{CAS}$ and $\overline{RAS}$ are then switched high to end the operation. A new cycle cannot begin until the precharge period has elapsed.

Random write operations follow the same sequence of events, except that the $\overline{WE}$ line is low for some portion of the cycle. If the data to be written is available early in the cycle, it will usually be convenient to simply have $\overline{WE}$ low for the whole write operation.

Sequential Read and Write operations at the same location can be designed to save time because re-addressing is not necessary. A read/write cycle holds $\overline{WE}$ high until a valid read is established and then strobes new data in with the falling edge of $\overline{WE}$.

After the power is first applied to the device, the internal circuit requires execution of at least eight initialization cycles which exercise $\overline{RAS}$ before valid memory accesses are begun.

### ADDRESSING

14 address bits are required to select one location out of the 16,384 cells in the memory. Two groups of 7 bits each are multiplexed onto the 7 address lines and latched into the internal address registers. Two negative-going external clocks are used to control the multiplexing. The Row Address Strobe ($\overline{RAS}$) enters the row address bits and the Column Address Strobe ($\overline{CAS}$) enters the column address bits.

When $\overline{RAS}$ is inactive, the memory enters its low power standby mode. Once the row address has been latched, it need not be changed for successive operations within the same row, allowing high-speed page-mode operations.

Page-mode operations first establish the row address and then maintain $\overline{RAS}$ low while $\overline{CAS}$ is repetitively cycled and designated operations are performed. Any column address within the selected row may be accessed in any sequence. The maximum time that $\overline{RAS}$ can remain low is the factor limiting the number of page-mode operations that can be performed.

Multiplexed addressing does not introduce extra delays in the access path. By inserting the row address first and the column address second, the memory takes advantage of the fact that the delay path through the memory is shorter for column addresses. The column address does not propagate through the cell matrix as the row address does and it can therefore arrive somewhat later than the row address without impacting the access time.

### REFRESH

The Am9016 is a dynamic memory and each cell must be refreshed at least once every refresh interval in order to maintain the cell contents. Any operation that accesses a row serves to refresh all 128 cells in the row. Thus the refresh requirement is met by accessing all 128 rows at least once every refresh interval. This may be accomplished, in some applications, in the course of performing normal operations. Alternatively, special refresh operations may be initiated. These special operations could be simply additional conventional accesses or they could be "$\overline{RAS}$-only" cycles. Since only the rows need to be addressed, $\overline{CAS}$ may be held high while $\overline{RAS}$ is cycled and the appropriate row addresses are input. Power required for refreshing is minimized and simplified control circuitry will often be possible.

### DATA INPUT/OUTPUT

Data is written into a selected cell by the combination of $\overline{WE}$ and $\overline{CAS}$ while $\overline{RAS}$ is low. The later negative transition of $\overline{WE}$ or $\overline{CAS}$ strobes the data into the internal register. In a write cycle, if the $\overline{WE}$ input is brought low prior to $\overline{CAS}$, the data is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the cycle is a read/write cycle then the data set-up and hold times are referenced to the negative edge of $\overline{WE}$.

In the read cycle the data is read by maintaining $\overline{WE}$ in the high state throughout the portion of the memory cycle in which $\overline{CAS}$ is low. The selected valid data will appear at the output within the specified access time.

### DATA OUTPUT CONTROL

Any time $\overline{CAS}$ is high the data output will be off (after tOFF). The output contains either one or zero during read cycle after the access time has elapsed. Data remains valid from the access time until $\overline{CAS}$ is returned to the high state. The output data is the same polarity as the input data.

The user can control the output state during write operations by controlling the placement of the $\overline{WE}$ signal. In the "early write" cycle (see note 9) the output is at a high impedance state throughout the entire cycle.

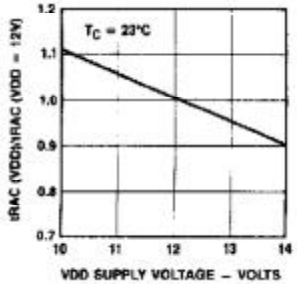
### POWER CONSIDERATIONS

$\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the Am9016 but overall system power is minimized if $\overline{RAS}$ is used for this purpose. The devices which do not receive $\overline{RAS}$ will be in low power standby mode regardless of the state of $\overline{CAS}$.

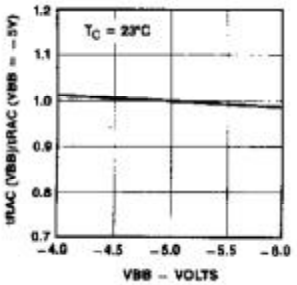
At all times the Absolute Maximum Rating Conditions must be observed. During power supply sequencing VBB should never be more positive than VSS when power is applied to VDD.

## TYPICAL CHARACTERISTICS

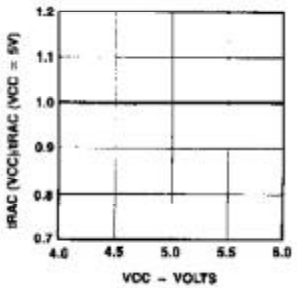
**Typical Access Time (Normalized) tRAC Versus VDD**



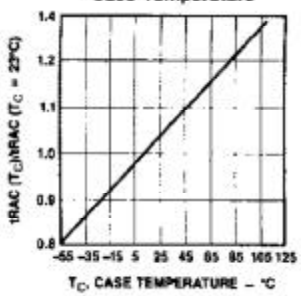

**Typical Access Time (Normalized) tRAC Versus VBB**



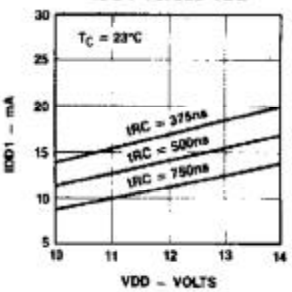

**Typical Access Time (Normalized) tRAC Versus VCC**



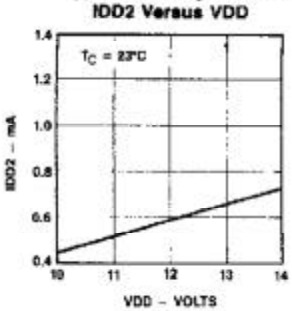

**Typical Access Time (Normalized) tRAC Versus Case Temperature**



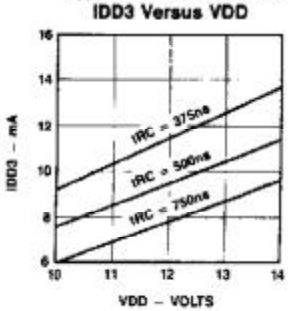

**Typical Operating Current IDD1 Versus VDD**



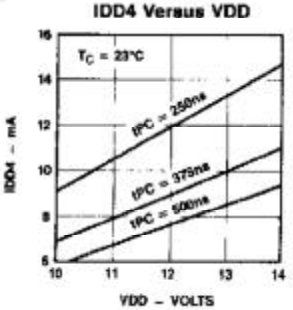

**Typical Standby Current IDD2 Versus VDD**



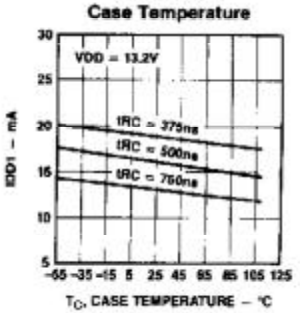

**Typical Refresh Current IDD3 Versus VDD**



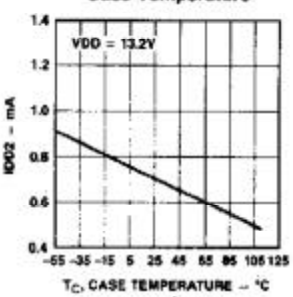

**Typical Page Mode Current IDD4 Versus VDD**



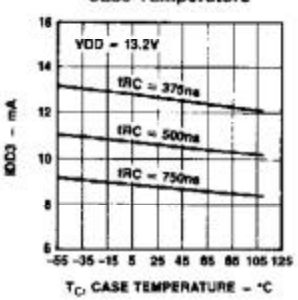

**Typical Operating Current IDD1 Versus Case Temperature**



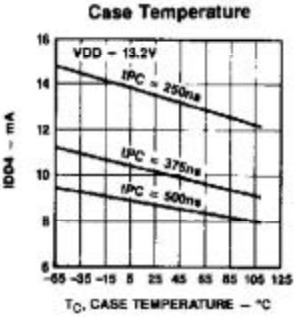

**Typical Standby Current IDD2 Versus Case Temperature**




**Typical Refresh Current IDD3 Versus Case Temperature**




**Typical Page Mode Current IDD4 Versus Case Temperature**

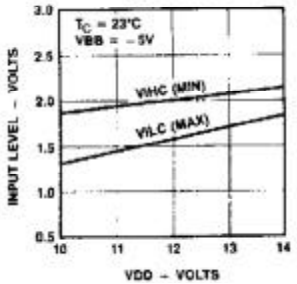



MOS-197

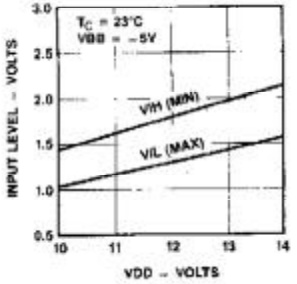
4

## TYPICAL CHARACTERISTICS (Cont.)

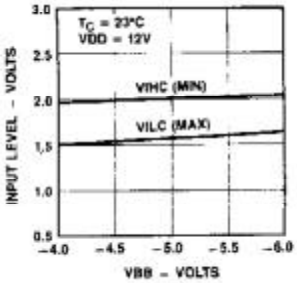
**Input Voltage Levels Versus VDD**



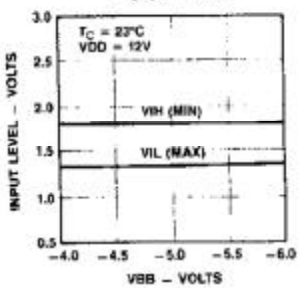

**Input Voltage Levels Versus VDD**



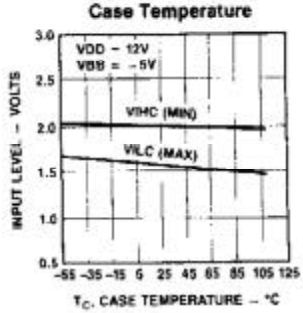

**Input Voltage Levels Versus VBB**



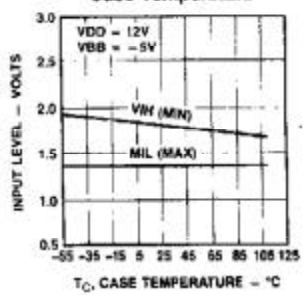

**Input Voltages Levels Versus VBB**



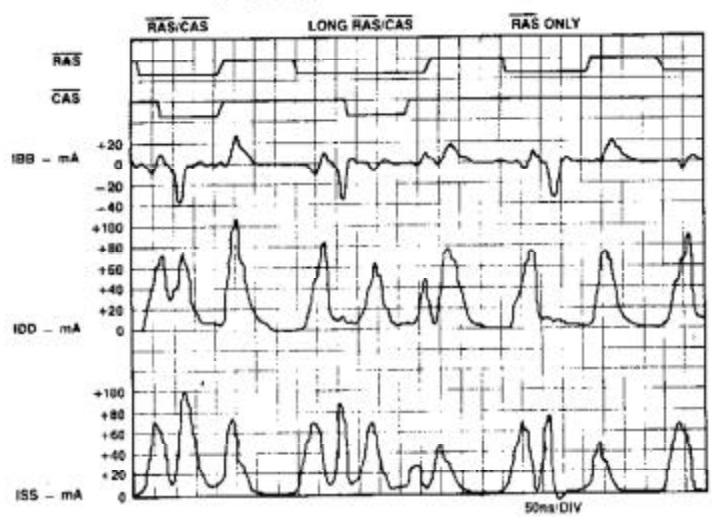

**Input Voltage Levels Versus Case Temperature**



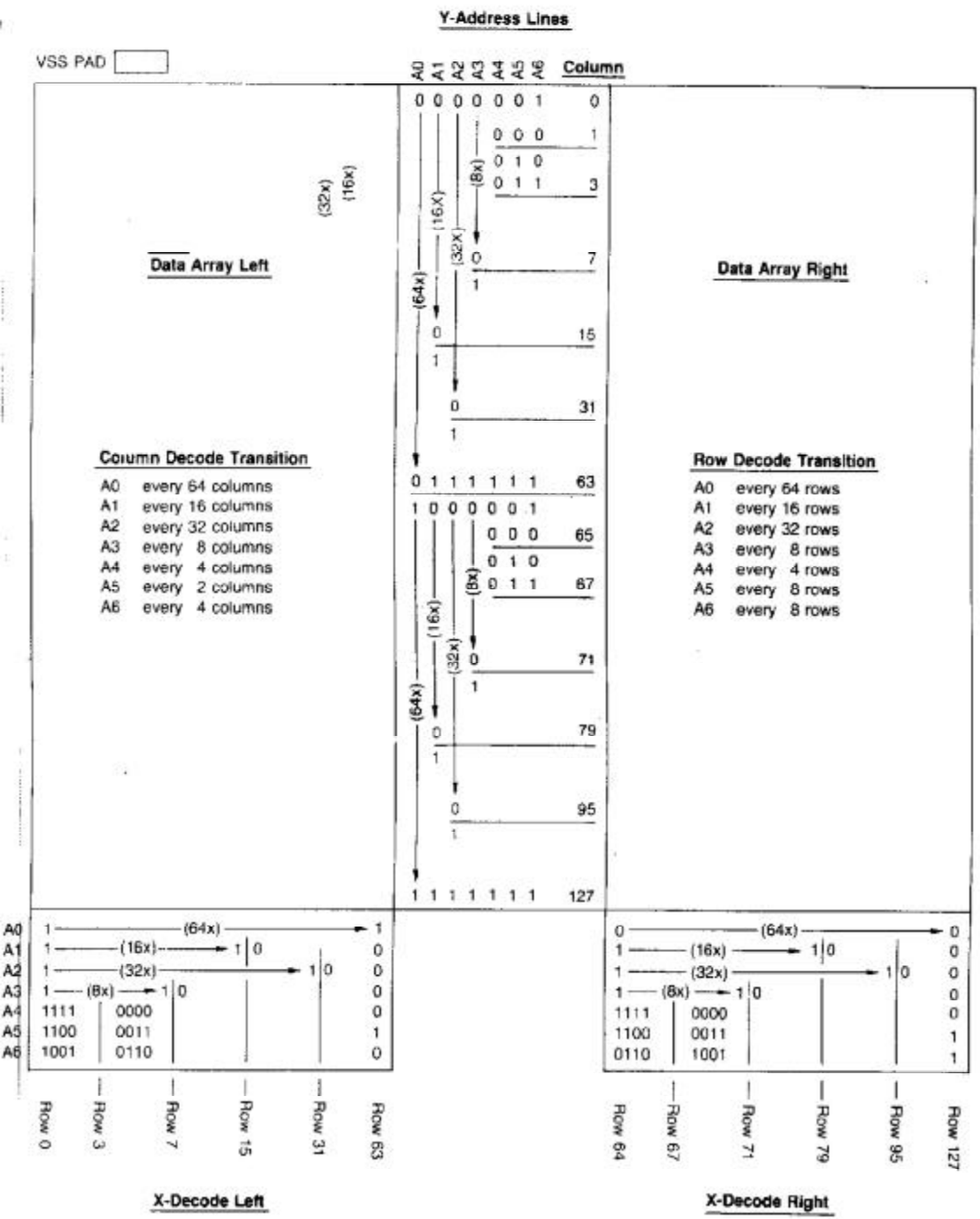

**Input Voltage Levels Versus Case Temperature**




## TYPICAL CURRENT WAVEFORMS




MOS-198



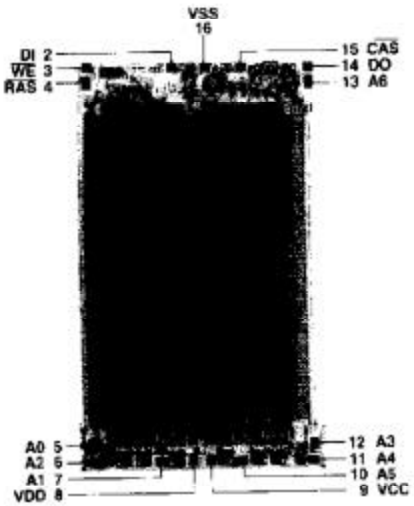

TOPOLOGICAL BIT MAP

4

## ORDERING INFORMATION

| Ambient Temperature | Package Type | Access Time | | | |
|---|---|---|---|---|---|
| | | 300ns | 250ns | 200ns | 150ns |
| 0°C ≤ $T_A$ ≤ +70°C | Hermetic DIP | AM9016CDC | AM9016DDC | AM9016EDC | AM9016FDC |
| | Molded DIP | AM9016CPC | AM9016DPC | AM9016EPC | AM9016FPC |
| | Chip-Pak | AM9016CLC | AM9016DLC | AM9016ELC | AM9016FLC |
| −55°C ≤ $T_A$ ≤ +85°C | Hermetic DIP | AM9016CDL | AM9016DDL | AM9016EDL | – |
| | Chip-Pak | AM9016CLL | AM9016DLL | AM9016ELL | |

## Metallization and Pad Layout




DIE SIZE 0.107" X 0.205"